7-MHz, 1.1-kW Demonstration of the New $E/F_{2,odd}$ Switching Amplifier Class

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***Abstract* – The first switching amplifier in the new $E/F_{2,odd}$ class belonging to the new E/F_x family of switching power amplifiers has been successfully demonstrated. This push/pull amplifier exhibits 1.1kW, 85% drain efficiency and 17dB gain at 7MHz. The amplifier uses low cost switching MOSFETs and fits in a small volume of only 900cm^3 including an integrated cooling fan.**

I. Introduction

As the popularity of wireless communications continues to grow, designers are forced to improve the performance of RF circuits while at the same time pushing to higher frequencies and consuming less power. To meet these requirements, highly efficient, high-frequency power amplifiers are needed.

Several switching amplifier topologies such as class-E and class-F have demonstrated high performance at RF frequencies [1,2], but even these classes have fundamental performance limitations [3,4]. Class-E amplifiers have highly peaked voltage and current waveforms, and can tolerate only a limited transistor output capacitance. Class-F amplifiers have better waveforms, but at the price of complex tuned circuits needed to supply open and short circuits to the alternating harmonics.

This paper reports the first amplifier belonging to the new E/F_x family proposed to address these limitations. This family allows the reduced circuit complexity of class-E with waveforms approaching the efficiency of inverse class-F [5], while at the same time absorbing the transistor output capacitance into the circuit as in class-E. Furthermore, the tolerance for large transistor output capacitance can be several times that of class-E for many amplifiers in this family, potentially allowing for higher frequency operation using the same transistor technology.

II. Theory of Operation

This section describes the design evolution from the general E/F_x family, to the demonstrated class-$E/F_{2,odd}$ class.

A. *The E/F_x Family*

The E/F_x family allows for a tradeoff between the simplicity of E and the performance of inverse F while permitting the output capacitance of the switching device to be absorbed into the circuit as in E. This family of zero-voltage switched (ZVS) amplifiers consist of those wherein the switching device is presented with an inductive load at the fundamental, short circuit at some subset of the odd harmonics, open circuit at some subset of the even harmonics, and capacitive impedance at the remaining untuned harmonics. The inductance of the fundamental frequency impedance is then adjusted to achieve ZVS conditions. To distinguish the individual members of this family, a subscript indicates which harmonics have been tuned. When all odd harmonics have been short-circuited, the subscript *odd* is used. In addition to the amplifier reported here, a monolithic CMOS 2.4GHz, 1.5W E/F_3 amplifier is being reported simultaneously [6].

B. *Class-E/F_{odd}*

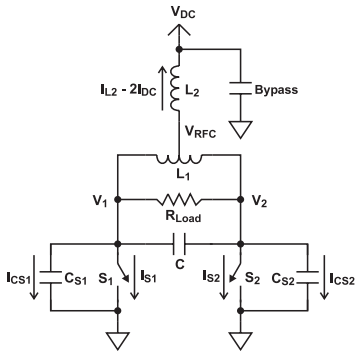

Fig. 1. Class E/F_{odd} ZVS amplifier realization, using symmetry to provide short-circuits at all odd harmonics.

Fig. 1 shows a topology to realize an E/F_{odd} amplifier, which is similar to a current-source class-D inverter [7]. It is possible with this simple push/pull circuit to provide virtual short-circuits at the odd harmonics to each switch while leaving the impedance seen by the switches at the even harmonics to be that of the switch output capacitance. Due to symmetry in the circuit, there is the additional benefit that the even harmonics are suppressed at the load, easing the task of filtering the output.

The waveforms for this class may be derived in the time domain. The resonator composed of L_1 and C is tuned near the fundamental frequency f_0, forcing the voltage across it to be a sinusoid at that frequency. The resonator is then detuned to have the required inductance at the fundamental frequency to achieve ZVS conditions. Since Kirchhoff's voltage law requires that the voltage across the resonator is the same as the difference between the switch voltages, and the switch

voltage is zero during the half-period when that switch is closed, the voltage across the each switch must then be half-sinusoidal. For the dc voltage of this waveform to equal the supply voltage V_{DC}, the peak voltage V_{pk} must be πV_{DC}:

$$V_1 = \begin{cases} 0 & 0 < \theta < \pi \\ -\pi V_{dc} \sin(\theta) & \pi < \theta < 2\pi \end{cases} \quad (1)$$

$$V_2 = \begin{cases} \pi V_{dc} \sin(\theta) & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \quad (2)$$

where the phase angle θ is $2\pi f_0 t$.

The currents through the (possibly nonlinear) output capacitors, each with small signal capacitance $C_S(V)$, may be found using the known switch voltages:

$$I_{CS1} = \frac{dQ}{dV_{CS1}} \frac{dV_{CS1}}{dt} = \begin{cases} 0 & 0 < \theta < \pi \\ -2\pi^2 f_0 V_{DC} C_S (-\pi V_{DC} \sin(\theta)) \cos(\theta) & \pi < \theta < 2\pi \end{cases} \quad (3)$$

$$I_{CS2} = \frac{dQ}{dV_{CS2}} \frac{dV_{CS2}}{dt} = \begin{cases} 2\pi^2 f_0 V_{DC} C_S (\pi V_{DC} \sin(\theta)) \cos(\theta) & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \quad (4)$$

If L_2 is large and conducts only dc current, we can notice that for each half-cycle one of the transistors is open circuited (and can be removed from the circuit) while the other is short circuited and conducts the excess current:

$$I_{S1} = \begin{cases} 2I_{dc} - I_{CS2} & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \quad (5)$$

$$I_{S2} = \begin{cases} 0 & 0 < \theta < \pi \\ 2I_{dc} - I_{CS1} & \pi < \theta < 2\pi \end{cases} \quad (6)$$

The waveforms for the E/F_{odd} class with linear output capacitance are depicted in Fig 2.

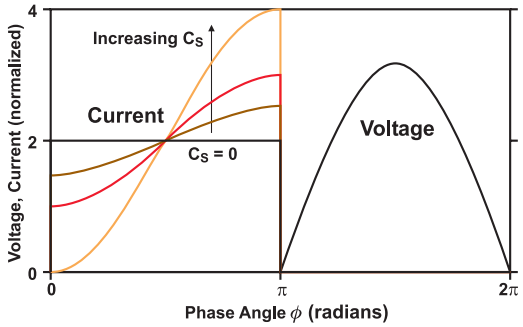

Fig. 2. Waveforms of E/F_{odd} for various values of C_S.

C. *Class-E/F$_{2,odd}$*

To reduce the RMS current, L_2 may be tuned to resonate with the output capacitors near the second harmonic, providing a near open-circuit to each switch at that frequency. This boosts the current in the first half of each transistor's conduction cycle while similarly reducing it in the second (Fig. 3).

By placing this inductor between the supply (ac ground) and the center tap of inductor L_1 (a virtual ground for the fundamental and odd harmonics), the desired resonance may be achieved while avoiding circulating currents at the fundamental and third harmonic. The resulting $E/F_{2,odd}$ amplifier waveforms are a modification of the E/F_{odd} result:

$$V_{L2} = \frac{V_{S1} + V_{S2}}{2} = \begin{cases} \frac{\pi}{2} V_{dc} \sin(\theta) & 0 < \theta < \pi \\ -\frac{\pi}{2} V_{dc} \sin(\theta) & \pi < \theta < 2\pi \end{cases} \quad (7)$$

$$I_{L2} = \frac{1}{L_2} \int V_{L2} dt = \begin{cases} \frac{\pi V_{dc}}{4\pi f_0 L_2} \left(1 - \frac{2\theta}{\pi} - \cos(\theta)\right) & 0 < \theta < \pi \\ \frac{\pi V_{dc}}{4\pi f_0 L_2} \left(1 - \frac{2(\theta - \pi)}{\pi} + \cos(\theta)\right) & \pi < \theta < 2\pi \end{cases} \quad (8)$$

$$I_{S1} = \begin{cases} 2I_{dc} - I_{CS2} - I_{L2} & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \quad (9)$$

$$I_{S2} = \begin{cases} 0 & 0 < \theta < \pi \\ 2I_{dc} - I_{CS1} - I_{L2} & \pi < \theta < 2\pi \end{cases} \quad (10)$$

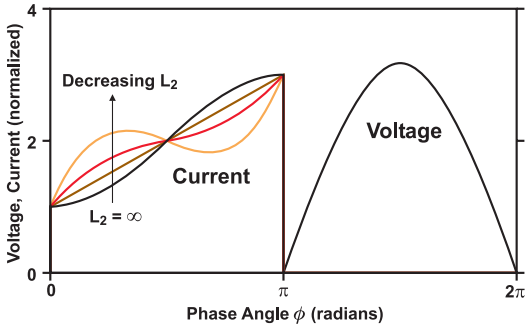

Fig. 3. Waveforms of $E/F_{2,odd}$ for various values of L_2.

A simple efficiency model indicates that this topology has the promise to achieve some of the efficiency benefits of inverse class-F while retaining the circuit simplicity of class-E. The voltage waveform is the same as inverse class-F, with a lower peak than class-E, and the RMS current is comparable to that of class-E. Classes E/F_{odd} and $E/F_{2,odd}$, can tolerate twice the output capacitance of a class-E for the same frequency and output power without negative switch current. Thus the frequency could be doubled from a class-E design without having to reduce the transistor size.

III. Circuit Design and Simulation

To verify the performance of the $E/F_{2,odd}$ amplifier class, a 7-MHz design with output power of 1kW was undertaken. For the active device, the STW20NB50 500V, 20A MOSFET from STMicroelectronics was chosen.

Since the circuit topology relies on a balanced load – not convenient for most applications – an output transformer is

used as a balun. The magnetizing inductance of this air-core transformer is used as the inductor L_1.

Modeling was performed using a simple switch model in PSPICE. The transistor's conductance characteristics were modeled as a switch in series with a resistance. To model the output capacitance, the drain-source capacitance was measured as a function of V_{ds} with $V_{gs} = 0$ and fit to a model consisting of a number of parallel varactors. The gate characteristics were not modeled.

In the simulation, the values of the tank components were adjusted to achieve ZVS conditions. To account for the parasitic package inductances, the simulation was performed with a 5nH inductance in series with each transistor. This results in a ringing transient superimposed on the voltage and current waveforms. This ringing is a result of the resonance between the two package inductors, the tank capacitor C, and the drain-source capacitor of the non-conducting transistor.

This ringing increases the RMS current through the switch, and it may cause the parasitic drain-source diode to conduct if the current becomes temporarily negative. Since both effects are undesirable, this ringing amplitude was reduced by lowering the loaded Q (quality factor) of the resonator consisting of L_1, C, and R_{Load} to a value of approximately 3.6. The second harmonic tuning also helps to keep the current positive by giving additional peaking in the early part of the current cycle where the ringing has the highest amplitude.

To avoid an unacceptably high third harmonic as a result of this low resonator Q, a third harmonic trap was added in series with the load. The final circuit is shown in Fig. 4.

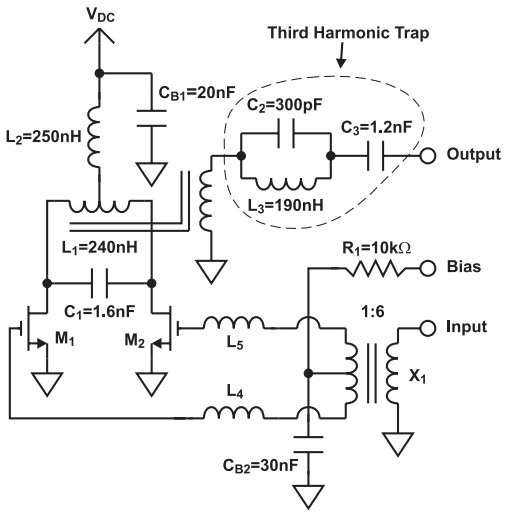

Fig. 4. Schematic of the class $E/F_{2,odd}$ amplifier reported here, with output balun and third harmonic trap.

Assuming passive component quality factors are 150, simulation results predict an output power of 1.4kW at 7MHz, with 90% drain efficiency using a 125V supply. The simulated waveforms are shown in Fig. 5.

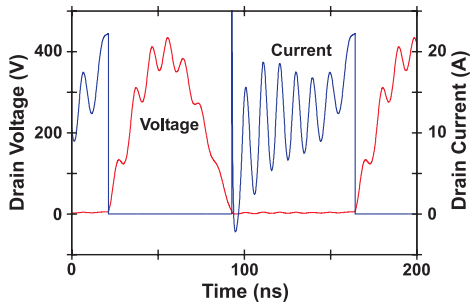

Fig. 5. Simulated waveforms for a single switch, including package inductance ringing.

IV. Measured Results

The amplifier is constructed on patterned FR4 circuit board. The transistors are directly mounted to an aluminum heatsink through holes cut in the circuit board, making for a compact and solid package. An integrated fan allows for continuous operation at this high power density. The resulting amplifier is small at approximately 11cm × 9cm × 9cm (including the fan), due to the lack of large inductors, made possible by using only parallel LC resonances in this topology.

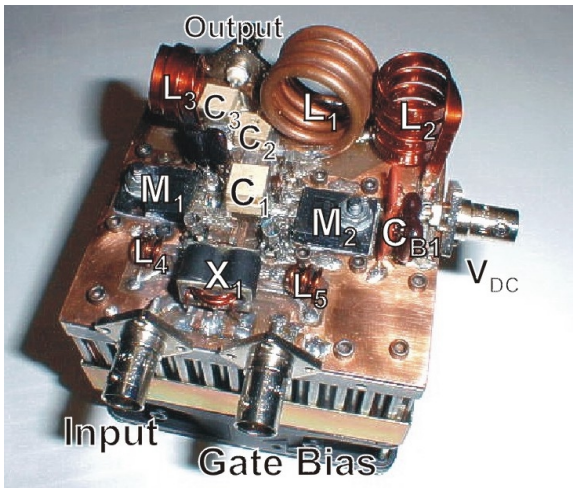

Fig. 6. Photograph of assembled amplifier.

Performance was measured using a Kenwood TS-850S RF Transceiver as the input source with a Bird 2kW, 30dB attenuator as the load. Power measurements were taken with Bird 4421 power meters equipped with Bird 4021 inline power sensors. The output spectrum was measured using an HP 8592A spectrum analyzer.

Fig. 7 shows the amplifier's measured drain efficiency as a function of drive power for several different output power levels. Fig. 8 shows efficiency and gain as a function of output power. The amplifier performs with similar efficiency over a wide range of drive powers, and the efficiency is

consistently high over a wide range of output powers, suggesting that the amplifier might be used effectively in an envelope elimination and restoration system [8]. The drain efficiency is around 87% up to 800W where it begins to degrade, probably as a result of transistor saturation at the higher current levels. Due to limitations of the power meters, measurements could only be taken up to 1.2 kW.

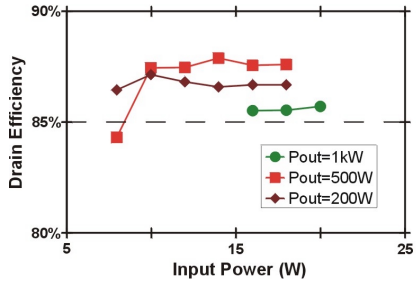

Fig. 7. Measured drain efficiency vs. input power.

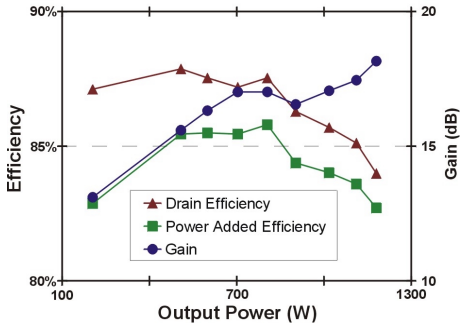

Fig. 8. Measured efficiency and gain vs. output power.

As should be expected with a switching amplifier, the gain increases with the output power since the input power remains relatively constant over the full range of output powers. The output power shows a very clear square law dependence on the supply voltage. The input voltage standing wave ratio (VSWR) is between 2:1 and 3:1 depending on output and input powers.

The second and third harmonics of the output spectrum are 33dB and 35dB below the fundamental respectively, and all other harmonics are at least 40dB below the fundamental. The second harmonic is high for a push/pull amplifier, probably the result of an imbalance in the impedances presented to the two transistors. We expect that this harmonic can be additionally suppressed by increasing the symmetry of the layout or adding compensation for the asymmetry. The third harmonic is present due to the output third-harmonic trap being imperfectly tuned, which should be correctable by additional tuning of this component.

The measured and simulated drain voltage waveforms for the two transistors are shown in Fig. 9. The ringing caused by the package inductance is visible.

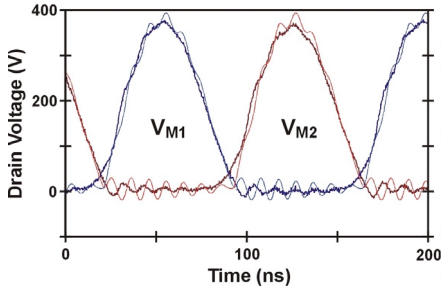

Fig. 9. Measured and simulated drain voltage waveforms.

V. Conclusion

The first amplifier from the new E/F_x family of switching amplifiers has been reported. In addition to demonstrating the feasibility of the new family, this E/$F_{2,odd}$ amplifier exhibits high efficiency at high power levels in an extremely compact design. It exhibits consistent performance over a wide range of input powers and DC voltages. The amplifier exhibits over 1.1 kW of output power with 85% drain efficiency and 17dB gain with a good agreement between simulation and measurements.

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